National Aviation University

Department of Electronics, Robotics, Monitoring and IoT Technologies

Course: “Analog and Digital Instrumentation”

Experiment 7

“Ramp-type digital voltmeter”

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LEARNING OBJECTIVE

- To study, construct and simulate the ramp-type digital voltmeter.

Theory

The operation principle of the Ramp-Type DVM is based on the measurement of the time which it takes for a linear ramp voltage to increase from zero level to the input voltage level, or to decrease from the level of the input signal to zero. This time is measured with an electronic counter and then result is displayed.

The block diagram of the Ramp-Type DVM is shown in Fig. 1. Conversion from a voltage to a time interval is illustrated by the waveform diagram of Fig. 2.

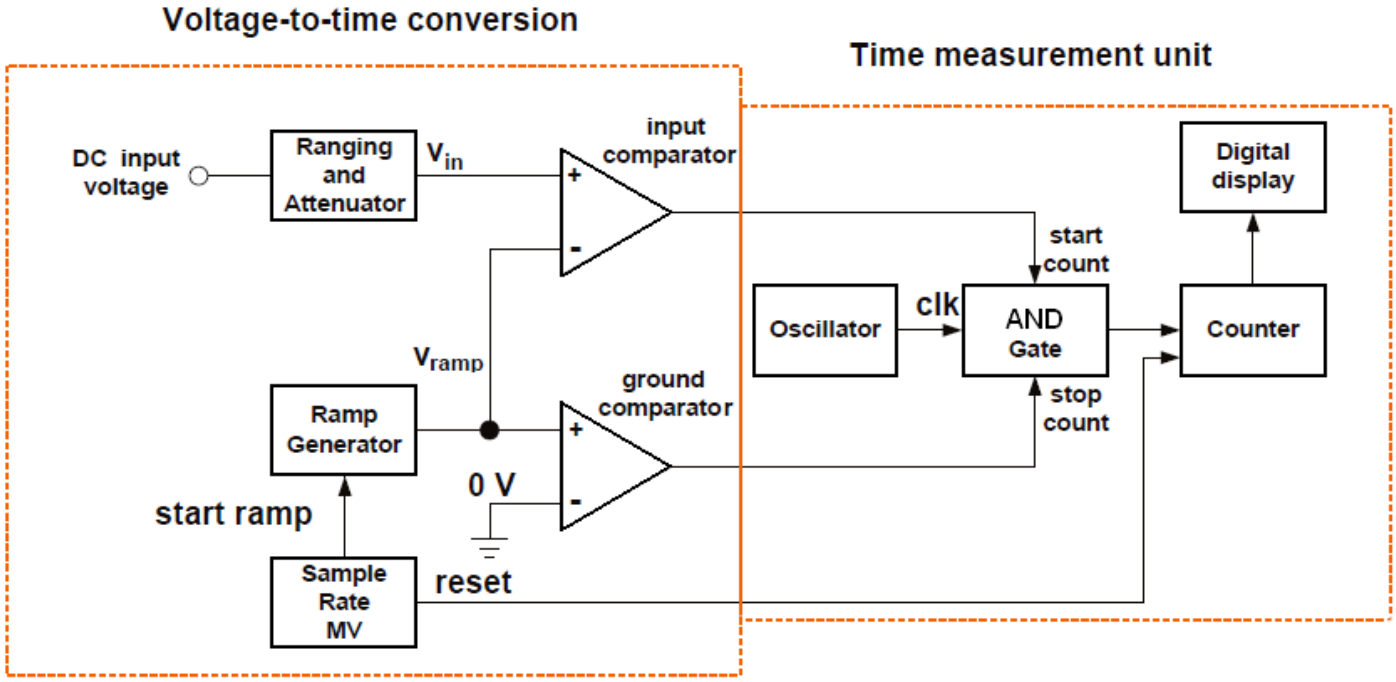

Figure 1: Block diagram of a ramp-type digital voltmeter

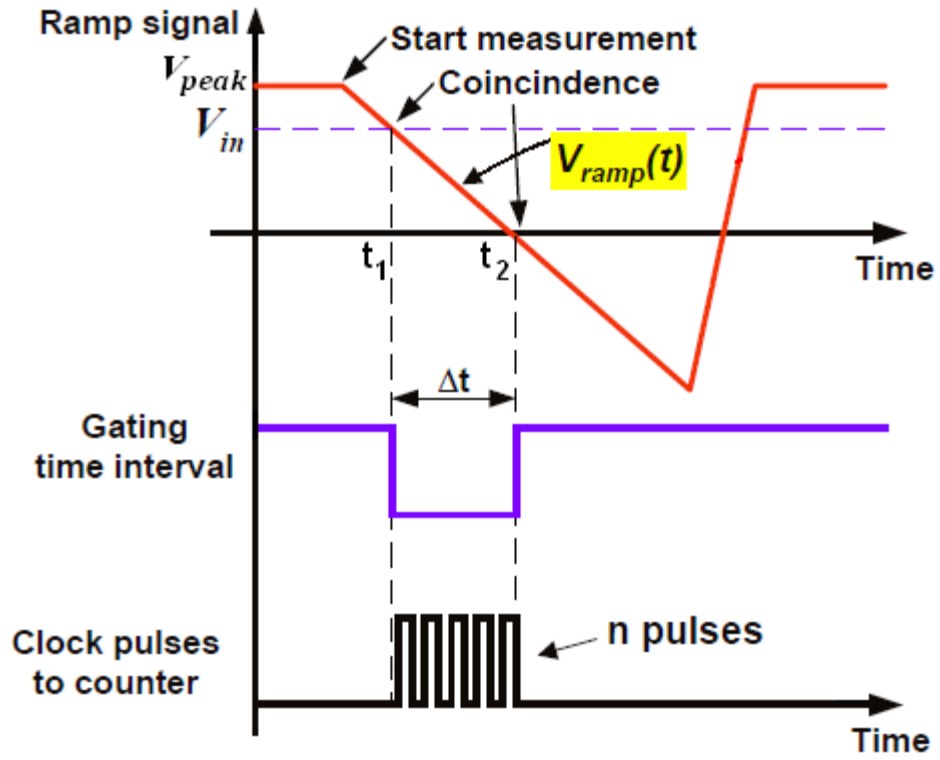

Figure 2: Voltage-to-time conversion using gated clock pulses

Consider the principle of operation of the Ramp-Type DVM. At the start of the measurement cycle a ramp voltage is generated. This voltage can be positive going or negative going. In Fig. 2, the negative-going ramp voltage is shown, which is continuously compared with the unknown input voltage into the input comparator. The ramp voltage is described by the following equation

$$V_{ramp}(t) = V_{peak} - m \times t$$

where m is the ramp voltage rate, $m = \Delta V / \Delta t$.

At the instance that the ramp voltage equals the unknown voltage,

$$V_{ramp}(t_1) = V_{in} = V_{peak} - m \times t_1$$

the input comparator output becomes logic 1. Since $V_{ramp} > 0$, then the output of the ground comparator is also logic 1 and the output of AND gate is equal to the output of the clock generator, $V_{AND} = V_{CLK}$.

The oscillator generates clock pulses which pass through the AND gate to the counter. This counter totalizes the number of pulses passed through the gate for

time $\Delta t = t_2 - t_1$. The ramp voltage continues to decrease with time until it finally reaches 0V (or ground potential)

$$V_{ramp}(t_2) = 0 = V_{peak} - m \times t_2$$

At this instance the ground comparator output becomes logic 0 and the AND gate output becomes also logic 0. The counter stops counting. The time interval Δt is given by

$$V_{ramp}(t_1) - V_{ramp}(t_2) = V_{in} - 0 = V_{peak} - m \times t_1 - V_{peak} + m \times t_2 = m \times (t_2 - t_1) = m \times \Delta t \Rightarrow \Delta t = \frac{V_{in}}{m}$$

If the period of the clock is *T*, then during the time interval Δt, the number of pulses is

$$n = \frac{\Delta t}{T}$$

The unknown voltage can now be represented as a linear function of *n*

$$V_{in} = m \times \Delta t = n \times m \times T \qquad (1)$$

As seen from the last equation, the accuracy of the ramp-type digital voltmeter depends on both the ramp rate and clock period. The magnitude of the input voltage is displayed on the digital display.

The sample rate multivibrator (MV) determines the rate at which the measurement cycles are initiated. The adjustment of this MV is provided by a front-panel control, marked “Rate”. The rate is usually from a few cycles per second to as high as 1000 or more.

The sample-rate circuit provides an initiating pulse for the ramp generator to start its next ramp voltage. At the same time, a reset pulse is generated which returns the counter to its zero state.

A comparator operation is illustrated in Fig. 3.

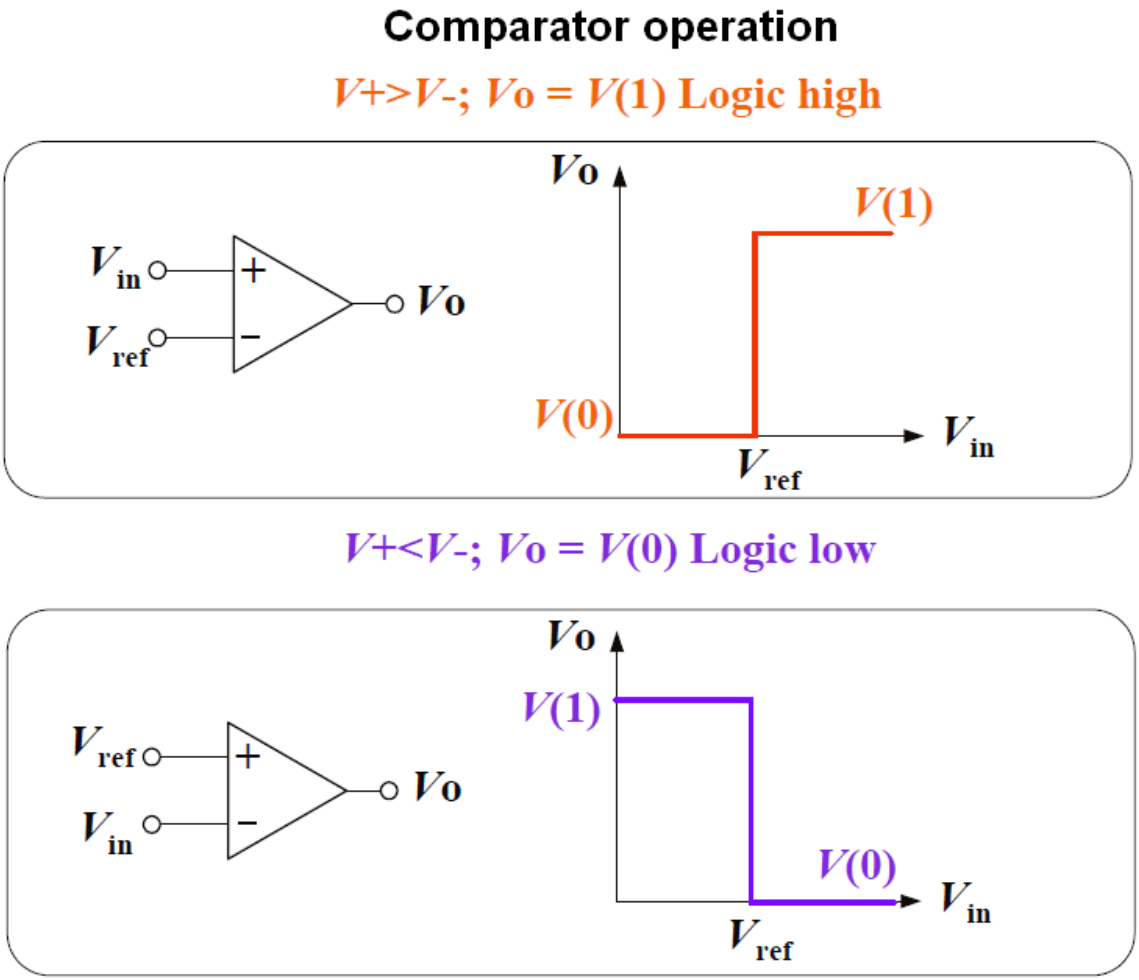

Figure 3: Illustration of a comparator operation

In Fig. 4, the time diagrams explaining the Ramp -Type DVM operation are shown. As seen, the number of pulses, n, is proportional to the duration of the gating time interval, Δt, which in turn is directly proportional to the magnitude of the input voltage, V_{in}.

The input and ground comparators can be realized with operational amplifier circuits. Figure 5 shows the circuit of the input comparator. The output voltage is given by

$$V_O = \begin{cases} -V_Z \Rightarrow V_{in} > V_{ramp} \\ -V_{D(ON)} \Rightarrow V_{in} < V_{ramp} \end{cases}$$

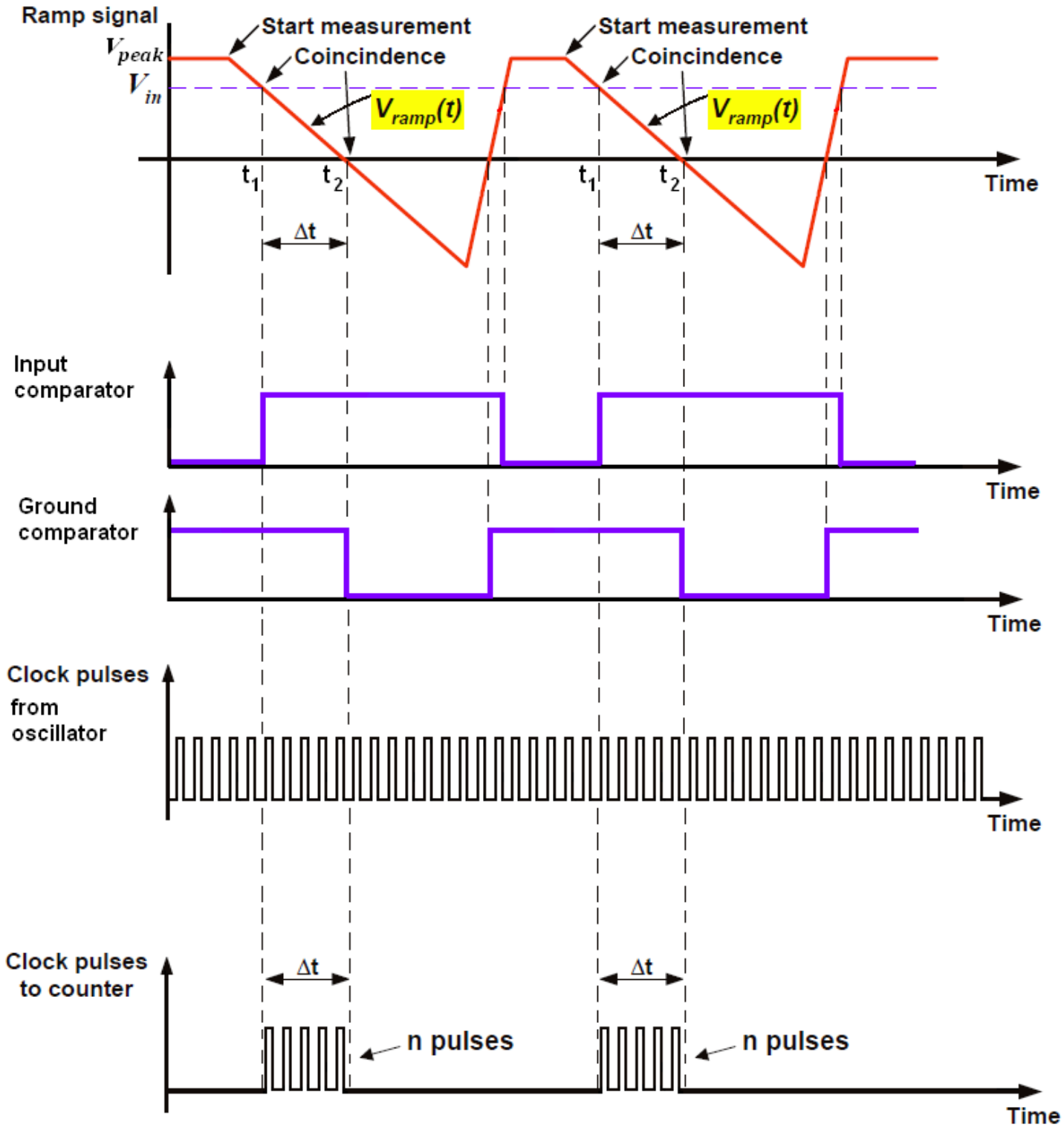

Figure 4: Time diagrams explaining the Ramp-Type DVM operation

The circuit of the input comparator was simulated by MULTISIM as shown in Fig. 6. The time diagrams explaining its operation are shown in Fig. 7 where V_Z=-3.0V

and V_D=0.6V. As seen, the output voltage, V_O, is equal to $-V_Z$=3V (logic 1) each time when $V_{in} > V_{ramp}$.

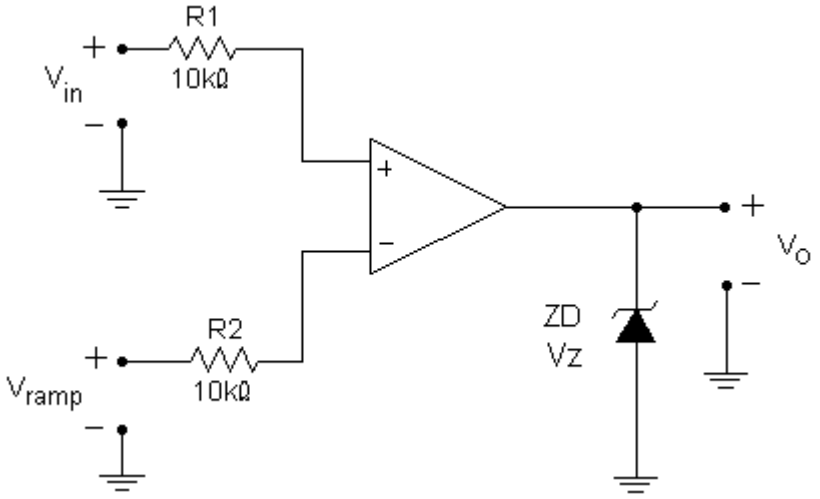

Figure 5: The input comparator circuit using an OPA and a Zener diode with a threshold voltage V_Z

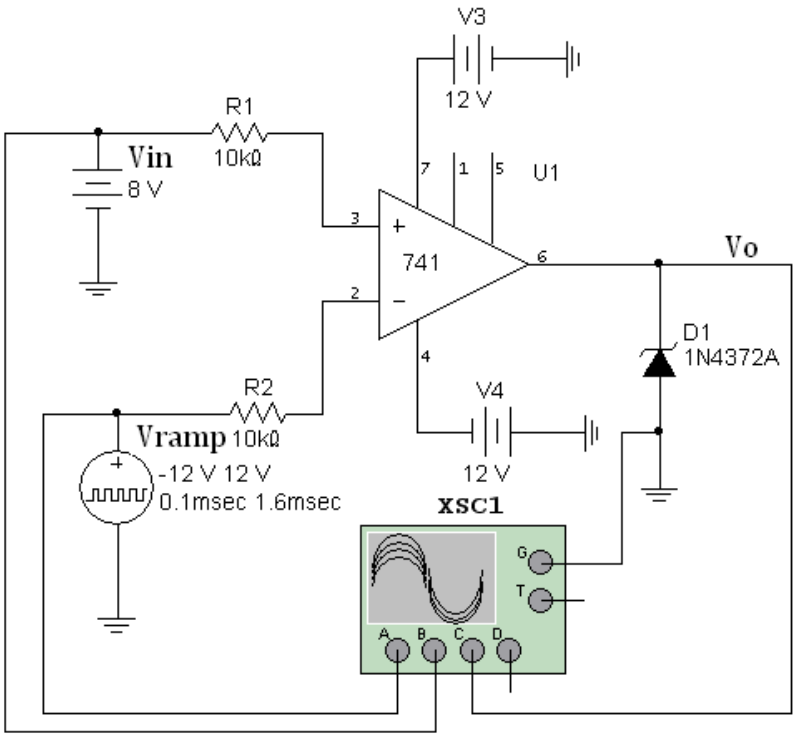

Figure 6: Simulated circuit of the input comparator with a Zener diode 1N4372A having V_Z=-3V and $V_{D(ON)}$=0.6V

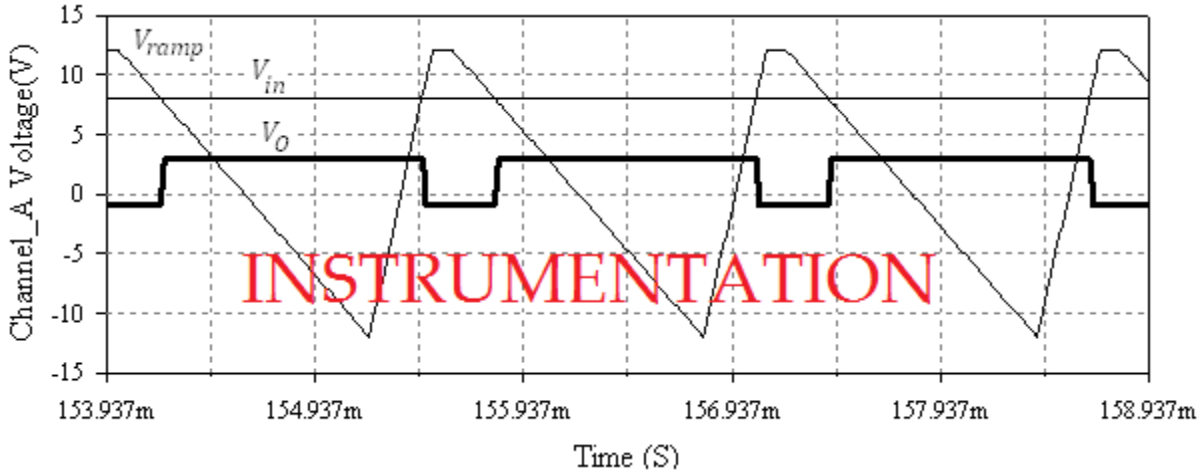

Figure 7: Time diagrams explaining the input comparator operation

The ground comparator circuit is shown in Fig. 8.

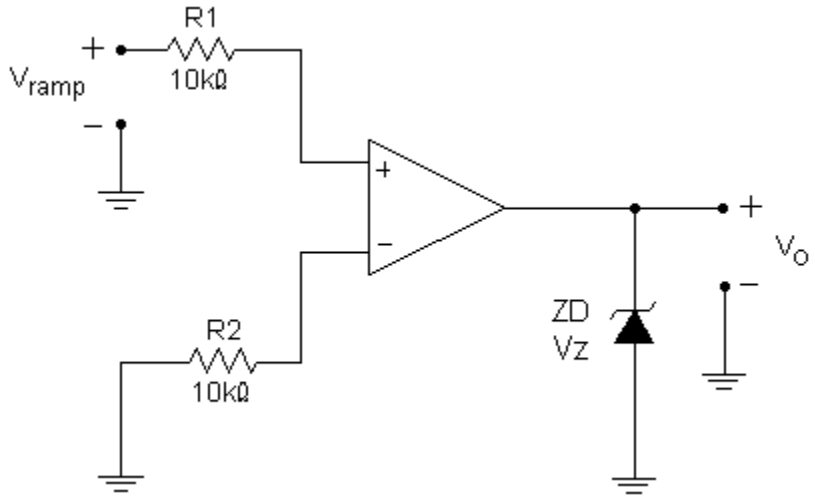

Figure 8: The ground comparator circuit using an OPA and a Zener diode

The output voltage of the ground comparator is given by

$$V_O = \begin{cases} -V_Z \Rightarrow V_{ramp} > 0 \\ -V_{D(ON)} \Rightarrow V_{ramp} < 0 \end{cases}$$

The ground comparator circuit was simulated by MULTISIM as shown in Fig. 9. The time diagrams explaining its operation are shown in Fig. 10. We can see that the output voltage, V_O, is equal to $-V_Z$=3V (logic 1) each time when V_{ramp} > 0V.

When V_{ramp} < 0V, the output voltage, V_O, is equal to $-V_{D(ON)}$= –0.6V, which corresponds to logic 0.

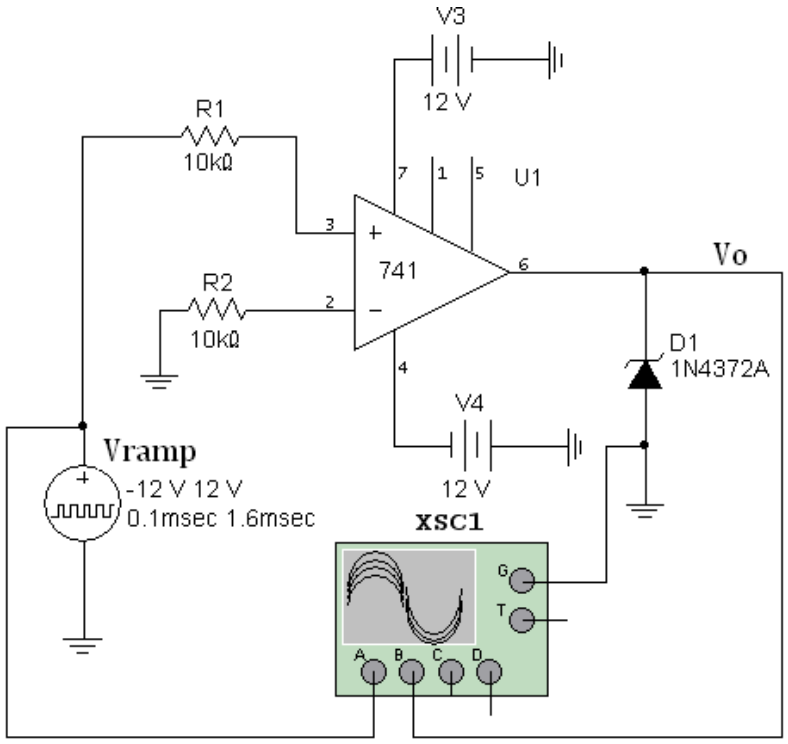

Figure 9: Simulated circuit of the ground comparator with a Zener diode 1N4372A having V_Z=-3V and $V_{D(ON)}$=0.6V

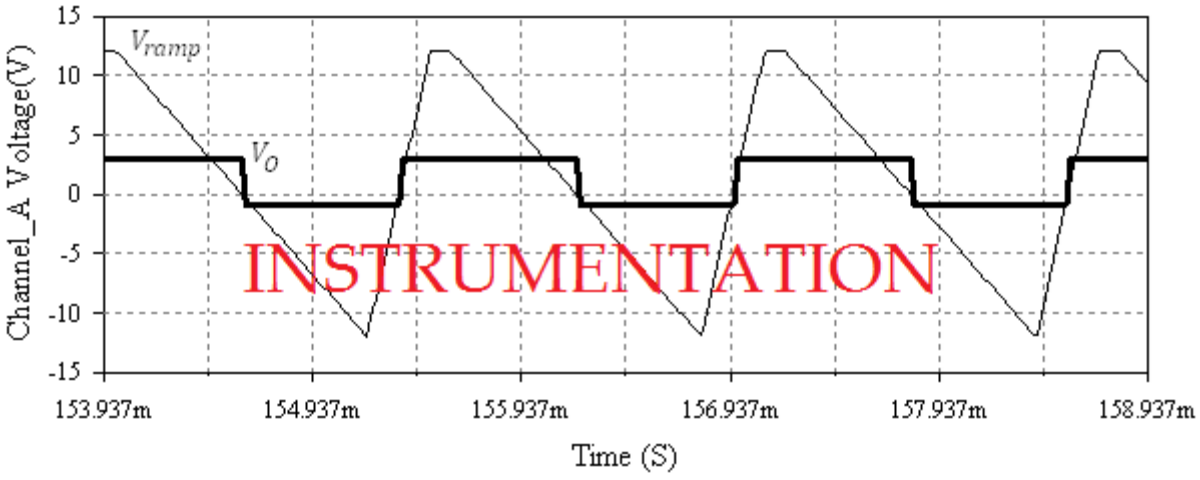

Figure 10: Time diagrams explaining the ground comparator operation

The ramp type DVM was simulated by MULTISIM as shown in Fig. 11. The counter and display circuits are not shown. The clock oscillator has frequency of 40 kHz.

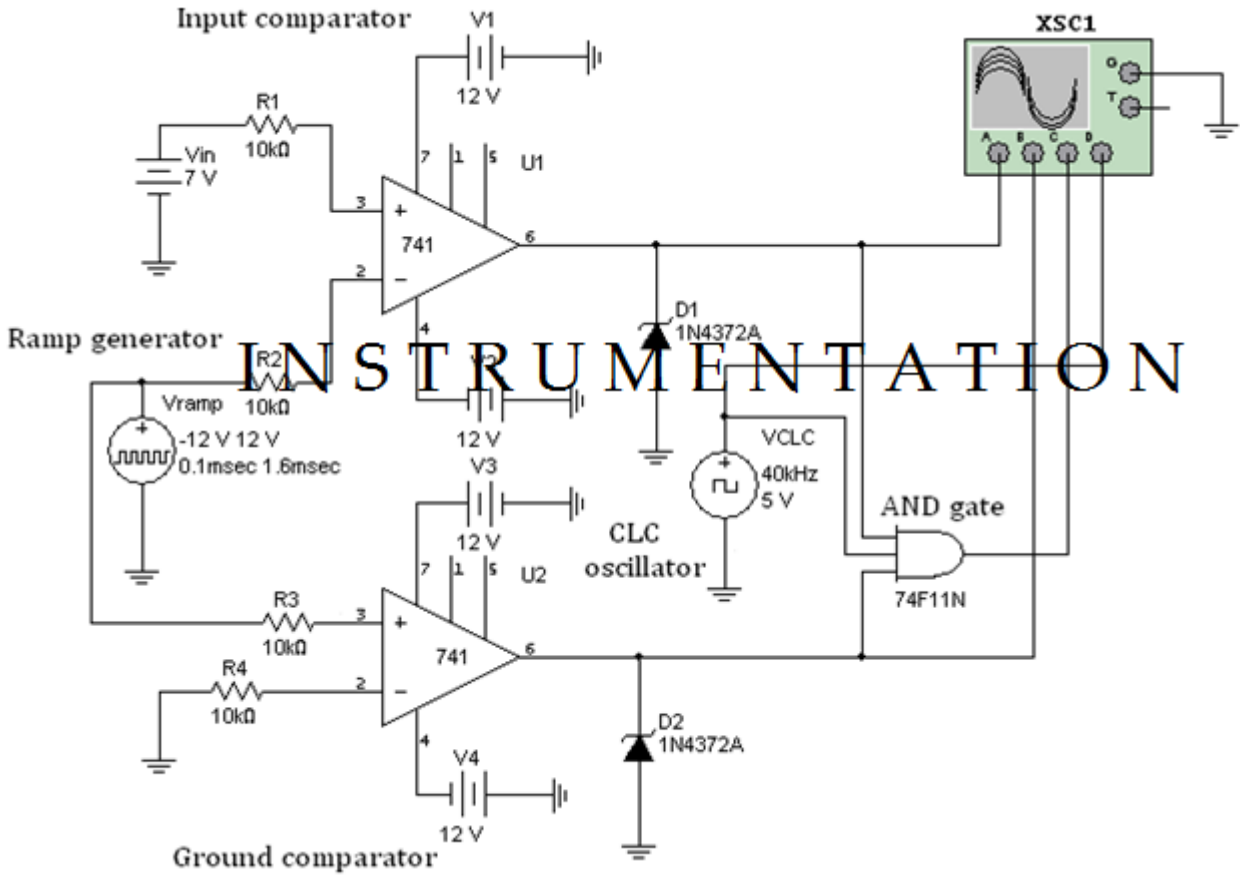

Figure 11: Ramp-type DVM simulated by MULTISIM

The time diagrams explaining the DVM operation are shown in Fig. 12. As seen, each time when the ground comparator voltage (V_{GR}) and input comparator voltage (V_{IN}) are at logic 1 at the same time, the output voltage of the AND gate (V_{AND}) is represented by a sequence of pulses. The number of pulses is proportional to the magnitude of the input voltage.

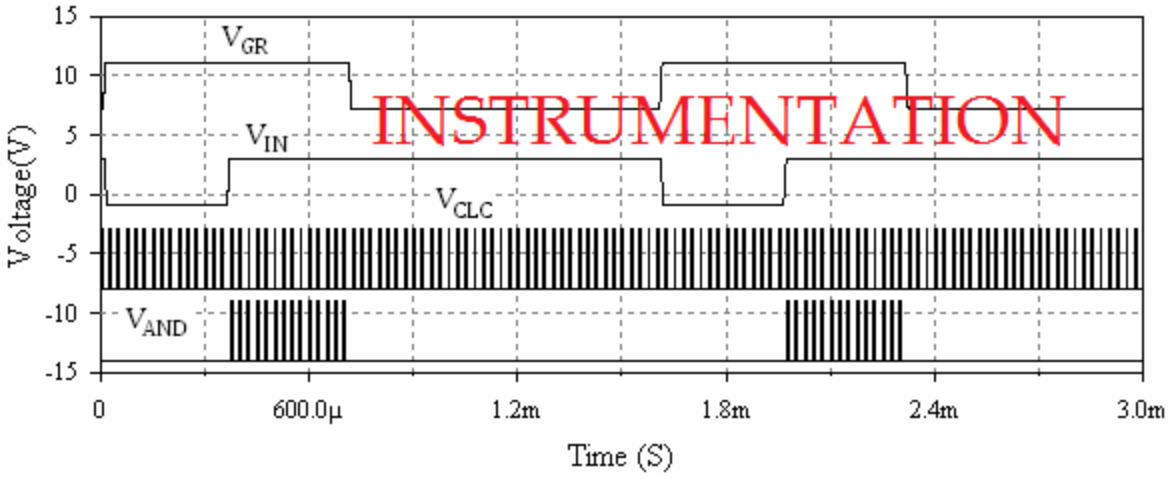

Figure 12: Simulated time diagrams

PROCEDURE:

1. Construct and simulate the circuit of the input comparator with a Zener diode 1N4372A having V_Z=-3V and $V_{D(ON)}$=0.6V as shown in Fig. 6.

2. Construct and simulate the circuit of the ground comparator with a Zener diode 1N4372A having V_Z=-3V and $V_{D(ON)}$=0.6V as shown in Fig. 9..

3. Construct and simulate the circuit of the ramp type DVM as shown in Fig. 11.