National Aviation University

Department of Electronics, Robotics, Monitoring and IoT Technologies

Course: "Fundamentals of Analog Electronics"

Experiment 5

"Common Source JFET Amplifier"

Prepared by prof. V. Ulansky

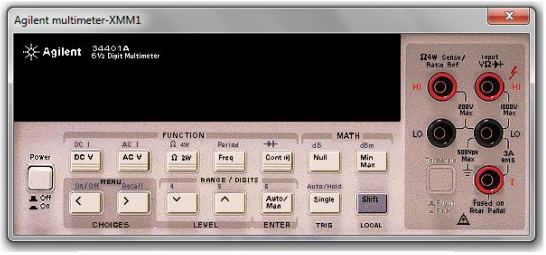
Kyiv

OBJECTIVES

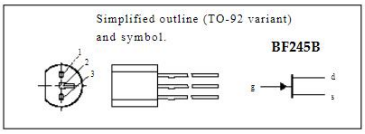
1. To measure the voltage and current gains of the CS JFET amplifier.
2. To measure the total harmonic distortion of the CS JFET amplifier.
3. To simulate the CS JFET amplifier using MULTISIM software.

EQUIPMENT

1. Digital multimeter: Agilent 34401A
2. Solderless breadboard: BB830T
3. Oscilloscope: Agilent 54622D
4. Sinusoidal generator
5. Power Supply: 20V
6. JFET: BF245B
7. Resistors: 1 × 1 kΩ, 1 × 67 kΩ, 1 × 4.7 kΩ, 1 × 20 kΩ, 1 × 147 Ω, 1 × 148 Ω
8. Capacitors: 1 × 47μF, 1 × 100 nF, 1 × 300 nF



PIN	SYMBOL	DESCRIPTION
1	d	drain
2	s	source
3	g	gate



Theory

The general circuit of a common-source (CS) JFET amplifier is shown in Fig. 1.

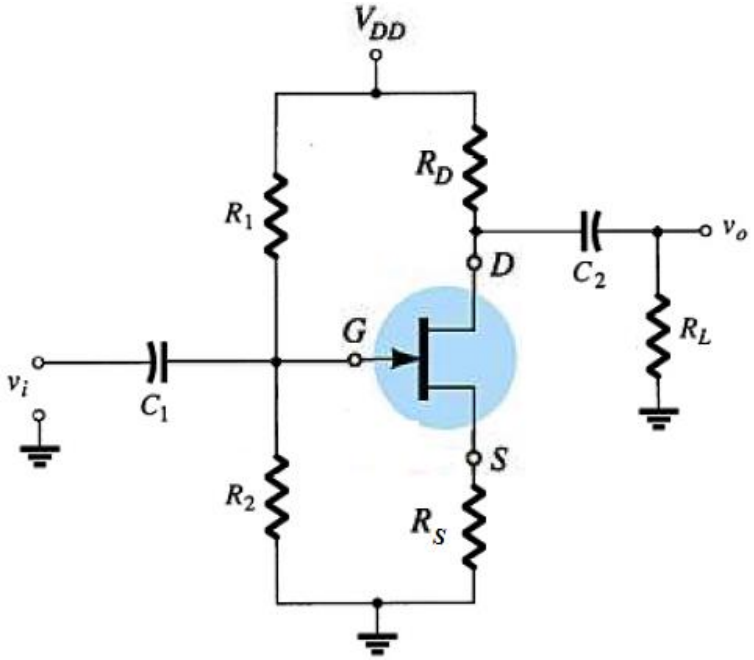


Fig. 1 Common-source JFET amplifier circuit

In Fig. 2, the *dc* equivalent circuit with the Thevenin equivalent of the bias circuit is shown.

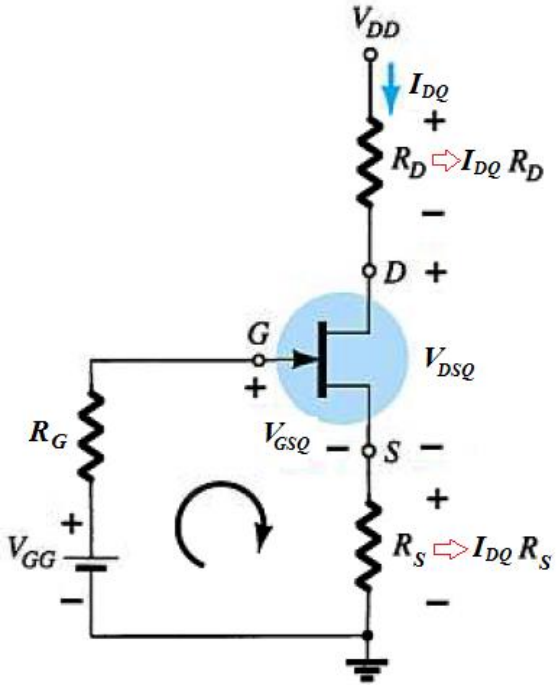


Fig. 2. A dc equivalent circuit of the CS amplifier

The Thevenin resistance and voltage are found as

$$R_G = R_1 \| R_2 \tag{1}$$

$$V_{GG} = V_{DD} \frac{R_2}{R_1 + R_2} \tag{2}$$

From Fig. 2 follows that there are three unknown variables I_{DQ}, V_{GSQ}, and V_{DSQ}. Therefore we need to have three *dc* equations. First equation we obtain from the gate-source loop:

$$V_{GG} = V_{GSQ} + I_{DQ} R_S \tag{3}$$

Notice that since the gate current is zero, a zero voltage drop exists across R_G. A second equation is found from the KVL equation in the drain-source loop as follows:

$$V_{DD} = V_{DSQ} + I_{DQ}(R_D + R_S) \tag{4}$$

The third *dc* equation necessary to establish the *Q*-point is found from the Shockley equation:

$$I_{DQ} = I_{DSS}(1 - V_{GSQ}/V_P)^2 \tag{5}$$

Notice that in order to reverse bias the *G-S* junction, voltage drop across R_S must be larger than voltage drop across R_2, i.e. V_{GG} ($V_{GG} < V_{RS}$).

The summary of the JFET biasing is shown in Fig. 3.

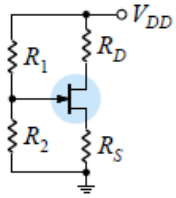
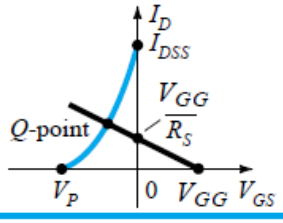
JFET Voltage-divider bias		$V_{GG} = \frac{R_2 V_{DD}}{R_1 + R_2}$ $V_{GSQ} = V_{GG} - I_{DQ} R_S$ $V_{DSQ} = V_{DD} - I_{DQ}(R_D + R_S)$	

Fig. 3 The summary of the JFET biasing

In Fig. 4, a small-signal equivalent circuit of the CS amplifier is shown. We assume that $r_{DS} >> R_D \| R_L$, so it can be neglected.

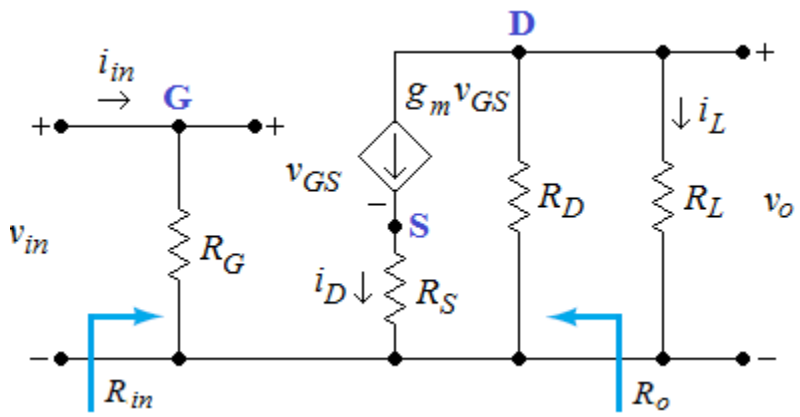


Fig. 4. A CS amplifier small-signal model

The voltage gain is

$$A_V = \frac{v_o}{v_{in}} \tag{6}$$

Writing a KVL equation around the gate circuit, we find

$$v_{in} = v_{GS} + i_D R_S \tag{7}$$

or

$$v_{in} = v_{GS} + g_m v_{GS} R_S = v_{GS}(1 + g_m R_S)$$

and finally

$$v_{GS} = \frac{v_{in}}{1 + g_m R_S} \tag{8}$$

The output voltage is $v_0 = i_L R_L$ or

$$v_o = -g_m v_{GS} R_L R_D / (R_D + R_L)$$

$$v_o = -g_m v_{GS} R_D \| R_L \tag{9}$$

Substituting v_{GS} from Eq, (8) into Eq. (9), gives

$$v_o = -g_m v_{in} \frac{R_D \| R_L}{1 + g_m R_S}$$

The voltage gain is

$$A_V = -\frac{g_m\left(R_D \| R_L\right)}{1 + g_m R_S} \tag{10}$$

Equation (10) can be rewritten in the following manner

$$A_V = -\frac{R_D \| R_L}{R_S + 1/g_m} \tag{11}$$

If R_S is bypassed by a large capacitor, then

$$A_V = -g_m\left(R_D \| R_L\right)$$

The voltage gain is increased in this case.

From Fig. 4 follows that

$$R_{in} = R_G = R_1 \| R_2$$

The current gain is found from the gain-impedance formula

$$A_i = A_V \frac{R_{in}}{R_L} = -\frac{R_D \| R_L}{R_S + 1/g_m} \times \frac{R_1 \| R_2}{R_L}$$

The output resistance is

$$R_0 = R_D$$

PROCEDURE

1. Construct the CS JFET amplifier circuit (see Fig. 5) on the solderless breadboard.
2. Turn on 20 V power supply.
3. Adjust the FREQUENCY control of signal generator so the output is 10 kHz sinusoidal waveform with 100 mV amplitude (70.7 mV rms).
4. Measure the voltage amplitude of the output voltage. Record the voltage measurement.
5. Measure the voltage amplitude going from the generator into the amplifier. Record the voltage measurement.

6. Use the formula $A_V = V_O/V_i$ to calculate the voltage gain. Record the voltage gain calculation.
7. Measure the rms current flowing from the generator into the amplifier ($I_{i,rms}$). Record the input current measurement.
8. Measure the rms current flowing through the 20-kΩ load resistor ($I_{L,rms}$). Record the load current measurement.
9. Use the formula $A_I = I_{L,rms}/I_{i,rms}$ to calculate the current gain. Record the current gain calculation.
10. Measure the total harmonic distortion (THD).

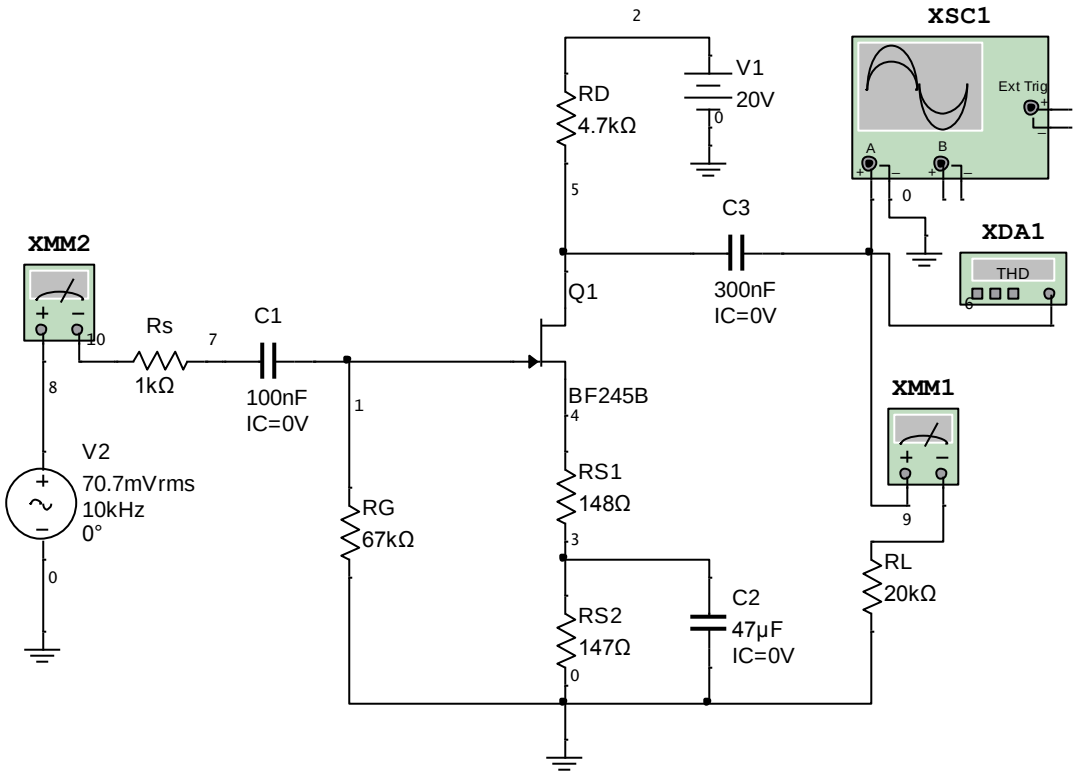


Fig. 5. Experimental CS JFET amplifier circuit diagram.

Reference

1. A.S. Sedra and K.S. Smith, "Microelectronic circuits", 5th ed., New York: Oxford University Press, 2004, 1283 p.